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Search History

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L21	L16 and ((pointer or indicator or tag) with (rom or eeprom or eprom))	1	L21
L20	(system-on-a-chip or system-on-chip or (system adj2 on adj2 chip))and((rom or eeprom or eprom or flash) same (configur$5 or initial$5))	40	L20
L19	((system-on-a-chip or system-on-chip or (system adj2 on adj2 chip))same (rom or eeprom or eprom or flash) same (configur$5 or initial$5))	5	L19
L18	l12 and (disabl$3 adj2 alias$3)	1	L18
L17	L16 and alias$3	19	L17
L16	(system-on-a-chip or system-on-chip or (system adj2 on adj2 chip))	291	L16
L15	l14 and ((multipl$5 or pluralit$3) with memor$3 with alias$3)	4	L15
L14	((rom or eeprom or eprom or flash) with alias$3)	70	L14
L13	L12 and l7	0	L13
L12	((rom or eeprom or eprom or flash) same alias$3)	249	L12
L11	l2 and ((rom or eeprom or eprom or flash) same alias$3)	0	L11
L10	l7 and ((rom or eeprom or eprom or flash) same alias$3)	0	L10
L9	l7 and alias$3	17	L9
L8	L7 and allegrucci	1	L8
L7	(system-on-a-chip or (system adj on adj chip))	159	L7
L6	L3 and allegrucci	0	L6
L5	L3 and peugh	0	L5
L4	l2 and (system-on-a-chip or (system adj on adj chip))	1	L4
L3	l1 and (system-on-a-chip or (system adj on adj chip))	13	L3
L2	((711/103)!.CCLS.)	572	L2
L1	((711/$)!.CCLS.)	13874	L1

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(system-on-chip or system-on-a-chip or (system<near/2>on<near/2>chip))

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Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Low power system on chip implementation scheme of digital filtering cores**
Zwyssig, E.P.; Erdogan, A.T.; Arslan, T.;
Low Power IC Design (Ref. No. 2001/042), IEE Seminar on , 2001
Page(s): 5/1 -5/9

[Abstract] [PDF Full-Text (460 KB)] **IEE CNF**

2 **Developing system-on-chip experience in a higher education environment**
Portero, A.; Dent, Donald.J.;
Systems on a Chip (Ref. No. 2000/110), IEE Workshop on , 2000
Page(s): 12/1 -12/13

[Abstract] [PDF Full-Text (816 KB)] **IEE CNF**

3 **Aspects of dynamically reconfigurable logic**
Lysaght, P.;
Reconfigurable Systems (Ref. No. 1999/061), IEE Colloquium on , 1999
Page(s): 1/1 -1/5

[Abstract] [PDF Full-Text (340 KB)] **IEE CNF**

4 **Systems-on-chip: what are their limits?**
Roza, E.;
Systems on a Chip (Ref. No. 1999/133), IEE Colloquium on , 1999
Page(s): 1/1 -1/6

[Abstract] [PDF Full-Text (296 KB)] **IEE CNF**

5 **Emerging standards for manufacturing test of system-on-chip design**
Downey, D.; Lysaght, P.;
Systems on a Chip (Ref. No. 1999/133), IEE Colloquium on , 1999
Page(s): 10/1 -10/7

[Abstract] [PDF Full-Text (300 KB)] **IEE CNF**

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6 **Re-usable cores for DSP systems-on-chip applications**
McCanny, J.V.;
Signal Processing in 2000 (Ref. No. 1999/106), IEE Colloquium on , 1999
Page(s): 3/1 -3/19

[Abstract] [PDF Full-Text (296 KB)] **IEE CNF**

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7 **Data compression for system-on-chip testing using ATE**
Karimi, F.; Meleis, W.; Navabi, Z.; Lombardi, F.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on , 2002
Page(s): 166 -174

[Abstract] [PDF Full-Text (912 KB)] **IEEE CNF**

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8 **Managing power and performance for system-on-chip designs using voltage islands**
Lackey, D.E.; Zuchowski, P.S.; Bednar, T.R.; Stout, D.W.; Gould, S.W.; Cohn, J.M.;
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on , 2002
Page(s): 195 -202

[Abstract] [PDF Full-Text (629 KB)] **IEEE CNF**

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9 **On-chip interconnects for next generation system-on-chips**
Brinkmann, A.; Niemann, J.-C.; Hehemann, I.; Langen, D.; Porrmann, M.; Ruckert, U.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 2002
Page(s): 211 -215

[Abstract] [PDF Full-Text (461 KB)] **IEEE CNF**

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10 **Fast system-level design space exploration for low power configurable multimedia systems-on-chip**
Polloni, F.; Mazzoni, L.; Di Matteo, S.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 2002
Page(s): 150 -154

[Abstract] [PDF Full-Text (418 KB)] **IEEE CNF**

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11 **Configurable systems-on-chip (CSoC)**
Becker, J.;
Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on , 2002
Page(s): 379 -384

[Abstract] [PDF Full-Text (719 KB)] **IEEE CNF**

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12 **A study on communication issues for systems-on-chip**
Zeferino, C.A.; Kreutz, M.E.; Carro, L.; Susin, A.A.;
Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on , 2002
Page(s): 121 -126

[Abstract] [PDF Full-Text (275 KB)] **IEEE CNF**

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13 **An all-digital phase-locked loop for high-speed clock generation**
Ching-Che Chung; Chen-Yi Lee;
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 3 , 2002
Page(s): 679 -682

[Abstract] [PDF Full-Text (453 KB)] **IEEE CNF**

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14 **A CAD tool for system-on-chip placement and routing with free-space optical interconnect**
Chung-Seok Seo; Chatterjee, A.;
Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE International Conference on , 2002
Page(s): 24 -29

[Abstract] [PDF Full-Text (789 KB)] **IEEE CNF**

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15 **Legacy systemC Co-simulation of multi-processor systems-on-chip**
Benini, L.; Bertozzi, D.; Bruni, D.; Drago, N.; Fummi, F.; Poncino, M.;
Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE International Conference on , 2002
Page(s): 494 -499

[Abstract] [PDF Full-Text (390 KB)] **IEEE CNF**

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(system-on-chip or system-on-a-chip or (system<near/2>on<near/2>chip)) and alias*

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Efficient construction of aliasing-free compaction circuitry**
Sinanoglu, O.; Orailoglu, A.;
Micro, IEEE , Volume: 22 Issue: 5 , Sep/Oct 2002
Page(s): 82 -92

[Abstract] [PDF Full-Text (300 KB)] **IEEE JRN**

2 **Compaction schemes with minimum test application time**
Sinanoglu, O.; Orailoglu, A.;
Asian Test Symposium, 2001. Proceedings. 10th , 2001
Page(s): 199 -204

[Abstract] [PDF Full-Text (610 KB)] **IEEE CNF**

3 **Space and time compaction schemes for embedded cores**
Sinanoglu, O.; Orailoglu, A.;
Test Conference, 2001. Proceedings. International , 2001
Page(s): 521 -529

[Abstract] [PDF Full-Text (818 KB)] **IEEE CNF**

4 **Empirical bounds on fault coverage loss due to LFSR aliasing**

Debany, W.H.; Gorniak, M.J.; Daskiewich, D.E.; Macera, A.R.; Kwiat, K.A.; Dussault, H.B.;
VLSI Test Symposium, 1992. '10th Anniversary. Design, Test and Application: ASICs and Systems-on-a-Chip', Digest of Papers., 1992 IEEE , 7-9 Apr 1992
Page(s): 143 -148

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

5 **Effective concurrent test for a parallel-input multiplier using modulo 3**

Debany, W.H.; Macera, A.R.; Daskiewich, D.E.; Gorniak, M.J.; Kwiat, K.A.; Dussault, H.B.;

VLSI Test Symposium, 1992. '10th Anniversary. Design, Test and Application: ASICs and Systems-on-a-Chip', Digest of Papers., 1992 IEEE , 7-9 Apr 1992

Page(s): 280 -285

[Abstract] [PDF Full-Text (404 KB)] IEEE CNF

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6 **Recent advances in BIST**

Gupta, S.K.;

VLSI Test Symposium, 1992. '10th Anniversary. Design, Test and Application: ASICs and Systems-on-a-Chip', Digest of Papers., 1992 IEEE , 7-9 Apr 1992

Page(s): 235 -240

[Abstract] [PDF Full-Text (448 KB)] IEEE CNF

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(multipl* or pluralit*)<sentence>(memory or memories)<sentence>alias*

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Multi-pattern real-valued spectral associative memories**
Spencer, R.G.;
Neural Networks, 2001. Proceedings. IJCNN '01. International Joint Conference on , Volume: 2 , 2001
Page(s): 1180 -1185 vol.2

[Abstract] [PDF Full-Text (624 KB)] **IEEE CNF**

2 **Notes on multiple input signature analysis**
Kameda, T.; Pilarski, S.; Ivanov, A.;
Computers, IEEE Transactions on , Volume: 42 Issue: 2 , Feb 1993
Page(s): 228 -234

[Abstract] [PDF Full-Text (704 KB)] **IEEE JRN**

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